AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

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that deuterium treatment will improve both programming and erasing in order to reduce random bit data loss.

The Applicant asserts that it is not obvious that the degree of electron trapping required during write/erase operation is met by deuterium doping, based upon the references cited. The references do not have the same operation sequence.

FLASH memory requires multiple sets of voltages for programming, erase, and read operations. FLASH memory characteristics are degrading because of stress by both programming and erasing and not just by programming. FLASH memory employs digital and analog design concepts. The effect that deuterium has on these features is not addressed by the art cited by the Examiner and cannot be presumed based upon what has been claimed and described in the present invention.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6976 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 20 Separator 01 Reg. No. 37,650

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this ZO day of September, 2001.